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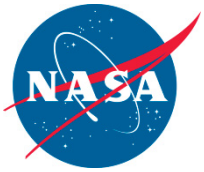

ASIC Fault Coverage Requirements for Space Application

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JPL Publication 11-10 11/11

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NASA Electronic Parts and Packaging (NEPP) Program
Office of Safety and Mission Assurance

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NASA WBS:
JPL Project Number: 104593
Task Number: 40.49.01.04

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This research was carried out at the Jet Propulsion Laboratory, California Institute of Technology, and was sponsored by the National Aeronautics and Space Administration Electronic Parts and Packaging (NEPP) Program.

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ABSTRACT

Testable designs of digital application-specific integrated circuits (ASICs) are essential to obtaining high-reliability “Hi-Rel” devices. At present, there are no quantifiable requirements in MIL-PRF-38535 or MIL-STD-883 for ASIC test and testability. The purpose of this task is to provide background information regarding ASIC test, testability, and fault coverage, along with a recommendation regarding the level of fault coverage needed to achieve a specified level of reliability for a specified mission duration.

1.0 INTRODUCTION

In the early 1980s when ASICs contained no more than 1,000 gates, the process of detecting defects in an integrated circuit (IC) was much easier. Simple ad hoc fault detection techniques were used along with a "bed-of-nails" test setup to probe points on the board. This worked fine for systems with components never having more than a couple dozen pins.

However, as device performance and complexity grew, so did packaging and board design. Boards began having a mixture of through-hole and surface mount devices, and they were placed on both sides of the board. The conventional bed-of-nails approach was no longer feasible.

In addition to limited access, achieving 100% fault coverage with these complex devices was also an issue. In a reasonable amount of time, designers could come up with enough functional stimulations to achieve about 80% fault coverage using conventional ad hoc fault detection methodologies [1]. However, in order to achieve 95% fault coverage, much more work was involved and this became prohibitively expensive with complex modern ICs. Time to develop test programs grew from 3–6 man-months in 1980 to 12–24 man-months in 1990 [2].

Manufacturing defects in integrated circuits (ICs) are simulated and treated during test according to a number of fault models: bridging fault model, open fault model, delay fault model, and the stuck-at fault model. These have been at the heart of ASIC testing since the 1950s [3]. Fault coverage is a measure of how many logic elements within the device are tested with the set of test vectors. Fault models strive to model everything that could go wrong during the manufacturing of an IC. For example, a defect in the oxide of a complementary metal-oxide semiconductor (CMOS) transistor could manifest itself as stuck-on, which would fall under the stuck-at fault model. Or if the defect does not cause a hard error, it may change the timing of the cell, which would be known as a delay fault. In a perfectly comprehensive IC test, 100% fault coverage would be achieved, meaning every possible fault manifestation of every gate and every transistor would be tested.

In the mid-1980s, the Joint Test Action Group (JTAG) was formed to examine the board-level test problem and alternative ways to achieve greater test fault coverage. Companies like IBM, Texas Instruments, and Philips were also working on the problem. The solution was called "boundary scan design" (an implementation of the "design for testability" [DFT] philosophy) and JTAG consolidated and formalized the work of these companies into an international standard called "IEEE Standard Test Access Port and Boundary-Scan Architecture," IEEE 1149.1, first published in April 1990.

2.0 DESIGN FOR TESTABILITY & FAULT COVERAGE

2.1 Design for Testability

Behind the IEEE 1149.1 standard is the concept of "design for testability" or "DFT." Instead of fully relying on external circuits to test an ASIC, DFT is a concept based around using built-in features of the circuit-under-test to assist the testing process. This comes at a cost to performance, design methodology, and chip size, but greatly simplifies the task of automatically generating test patterns and lowers costs.

2.2 Scan Design

The first major DFT implementation was "scan" design. The goal of scan design is to achieve near total controllability (ability to drive desired signals) and observability (ability to observe resulting outcomes). In scan design, every flip-flop in the circuit is enhanced with a multiplexing mechanism that allows for the circuit to operate in two different modes: normal and test. In normal mode, the circuit behaves as usual. In test mode, all the flip-flops are connected as a single shift register. The input of the chain is a single controllable point and its output is a single observable point. This is known as a "full scan," as all flip-flops in the circuit are scanned. This is time-and hardware-intensive, however, especially when the chip has a large number of flip-flops.

2.3 Boundary Scan Design

To address the time and expense issues with full-scan design, boundary scan design was formulated. Instead of enhancing every flip-flop with multiplexing mechanisms as is done in scan design, boundary scan adds a "boundary scan cell" next to each component pin. This way, the signals between the circuit-under-test and other components are monitored at the "boundary" of the device. These cells form a shift register around the device, and are connected to the internal chip logic as well as the package pins. Using this shift register, test vectors can be loaded into the flip-flops and data extracted. At the device level, the boundary-scan elements contribute nothing to the functionality of the internal logic. The boundary-scan path is independent of the function of the device. As in regular scan design, there are also normal and test modes in boundary scan. During normal operation, data passes between pins and internal chip logic as normal. In test mode, the boundary scan cells are active. By loading data into the boundary-scan cells, the boundary-scan cells can inhibit data flow to or from the input/output (I/O) pins.

Actual execution of boundary scan testing of an ASIC requires additional I/O pins and logic on the ASIC. IEEE 1149.1 defines the pins, logic, and external test tools required.

2.4 DFT, Fault Coverage, and Space Application

DFT and boundary scan standards can increase fault coverage while decreasing test time and costs, but the question remains of how much fault coverage is necessary to produce an ASIC reliable enough for space application.

For a given mission duration with x number of ASICs, what fault coverage is necessary to achieve 99% system reliability? How does defect level and die yield factor into this? Can a system of fifty ASICs operate for ten-years with 99% reliability? Is that even possible?

3.0 PROBABILITY OF ASIC FAILURE

The total probability of failure of an IC is equal to the total probability of failure due to both extrinsic and intrinsic failure mechanisms:

$$P_{FAILURE} = P_{FAILURE\text{-}EXTRINSIC} + P_{FAILURE\text{-}INTRINSIC}. \quad (1)$$

More specifically, for an ASIC, the total probability of failure is the sum of 1) probability of electrical failure (data upset) due to insufficient fault coverage (extrinsic failure mechanisms), 2) probability of random failure during useful life of the device (intrinsic failure mechanisms), and 3) probability of failure due to radiation effects:

$$P_{FAILURE/ASIC} = P_{DEFECT} + P_{RANDOM} + P_{RADIATION}. \quad (2)$$

However, the effect from radiation is not within the scope of this paper and will be removed from the equation. Any probabilities of failure presented in this paper can be added to radiation effects analysis separately. P_{DEFECT} is equal to the probability of having a defective device times the probability that the circuit activates one or more of its defects [4]:

$$P_{DEFECT} = DL(1 - FC) \quad (3)$$

where DL is the defect level and FC is the fault coverage. The Williams Model provides a relationship between these two quantities based on the ASIC vendor's die yield, Y [4]:

$$DL = 1 - Y^{1-FC}. \quad (4)$$

This formula was first published in the early 1980s and matched experimental data at the time very well. However, this model does not take into consideration correlated faults (detecting one fault may in fact be detecting many). In 1998, Willing and Helland updated this equation to the following [5]:

$$DL = \frac{(1-FC)(1-Y)e^{-(n_0-1)(FC)}}{Y+(1-FC)(1-Y)e^{-(n_0-1)(FC)}}. \quad (5)$$

"n_0" is the average number of faults on a faulty die and was determined at the time (1998) to be between 2.5 and 4.0. By substituting Equation 5 into Equation 3, P_{DEFECT} is in terms of fault coverage and yield:

$$P_{DEFECT} = \frac{(1-FC)^2(1-Y)e^{-(n_0-1)(FC)}}{Y+(1-FC)(1-Y)e^{-(n_0-1)(FC)}}. \quad (6)$$

As for P_{RANDOM}, the second factor in Equation 2, intrinsic reliability follows the logarithmic distribution during the "useful life" portion of the bathtub curve:

$$P_{RANDOM} = 1 - e^{-\lambda t} \quad (7)$$

where P_{RANDOM} is the probability of failure during time t (hours), and λ is the failure rate, (failures per hour). Substituting Equations 6 and 7 into Equation 2:

$$P_{FAILURE/ASIC} = \frac{(1-FC)^2(1-Y)e^{-(n_0-1)(FC)}}{Y+(1-FC)(1-Y)e^{-(n_0-1)(FC)}} + (1 - e^{-\lambda t}). \quad (8)$$

4.0 FAULT COVERAGE REQUIREMENTS

Equation 8 has five variables. Table 4-1 lists the practical ranges of values for those variables.

The goal of this paper is to determine what level of fault coverage is required to achieve a certain level of ASIC reliability. However, for a given level of fault coverage, there are four other dimensions to consider: die yield Y, average number of defects per defective die n_0, average failure rate λ, and mission duration t. In order to simplify analysis, variables need to be eliminated wherever possible by making assumptions for the values of these variables.

4.1 Assumptions

Because changing n_0 between 1 and 4 does not have order-of-magnitude changes on the total probability of failure, it will be defined as 3.0 (same as done by Willing and Helland). Varying die yield also has little impact, so Y is set at 0.75. This way, ASIC reliability only varies with FC and λ for a given mission length t.

The range of 1–50 FITs (failures in time, or failures per billion device hours) for λ comes from published reliability data of a space ASIC manufacturer [6]. Table 4-2 provides a summary of the values of Equation 8 variables used in this analysis.

It is also important to note that in real application, an ASIC will not be operating all 87,600 hours of a 10-year mission. However, in this analysis, 100% duty cycle is assumed for calculation simplicity.

4.2 Results

Figure 4-1 shows the probability of failure for a single ASIC ($P_{FAILURE/ASIC}$) versus fault coverage FC and useful life failure rate λ for a 10-year mission. This plot shows that for long mission lifetimes, probability of failure is more dependent on intrinsic failure rate λ than fault coverage.

To achieve 0.5% chance of failure (99.5% chance of success) for a single ASIC operating for 10 years, fault coverage must be better than 90% with λ = 50 FITs.

50 FITs and 90% fault coverage are not lofty goals. However, this result is for a single ASIC. Most systems have many ASICs and the failure rate is compounded.

Table 4-1. Practical ranges for Equation 8 variables.

Parameter	Practical Range of Values
FC	80%–99%
Y	50%–95%
n_0	2.5–4
λ	1–50 FITs
t	90 days–10 years

Table 4-2. Values of Equation 8 variables used in this analysis.

Parameter	Values
FC	80–99%
Y	75%
n_0	3.0
λ	1–50 FITs
t	90 days, 1 year, 3 years, 5 years, 10 years

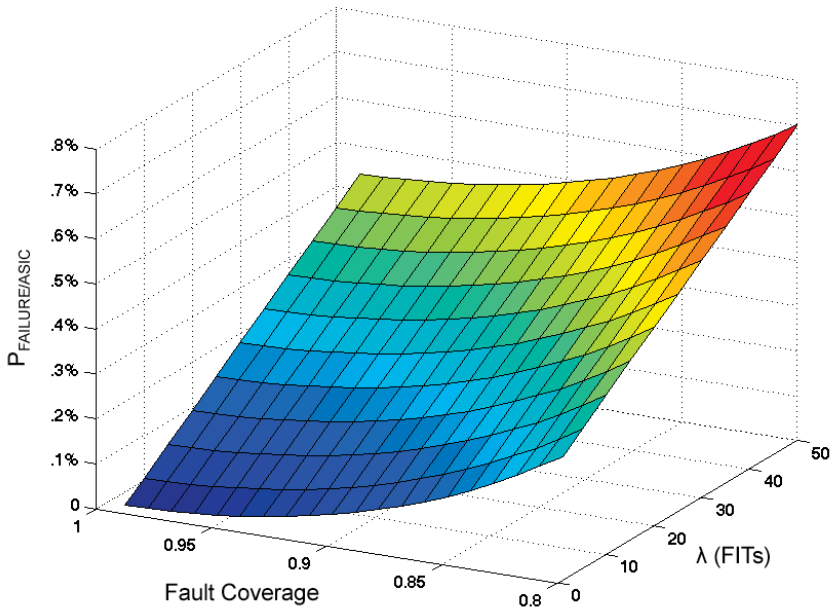

Figure 4-1. $P_{FAILURE/ASIC}$ versus fault coverage FC and useful life reliability λ for a 10-year mission.

In a system with *m* ASICs, the total probability of failure of the system is:

$$P_{FAILURE/SYS} = 1 - (1 - P_{FAILURE/ASIC})^m. \quad (9)$$

In the case of a 10-year mission with 50 ASICs, 99% fault coverage, and λ = 15 FITs, $P_{FAILURE/ASIC}$ is 0.1% and chance of system failure is:

$$P_{FAILURE/SYS} = 1 - (1 - 0.001)^{50} = 4.9\% \text{ chance of failure.} \quad (10)$$

For long missions with many ASICs, high levels of fault coverage and ultra-reliable ASIC processes are clearly required.

To achieve 1% chance of failure (99% chance of success) for 50 ASICs operating for 10 years, λ must be better than 3 FITs with 99% fault coverage.

Three FITs may sound impossible, but it is actually achievable with mature processes. 0.6 µm CMOS processes can have failure rates of <5 FITs. Less than 10 FITs is achievable down to 0.18 µm [6].

The following surface plots (Figures 4-2 through 4-5) are similar to Figure 4-1, but for 5-year, 3-year, 1-year, and 90-day missions. As the mission lifetimes get shorter, the less dependent $P_{FAILURE/ASIC}$ is on λ. For *t* = 1 year, λ has almost no effect on the probability of failure; failure rate is completely dominated by defects.

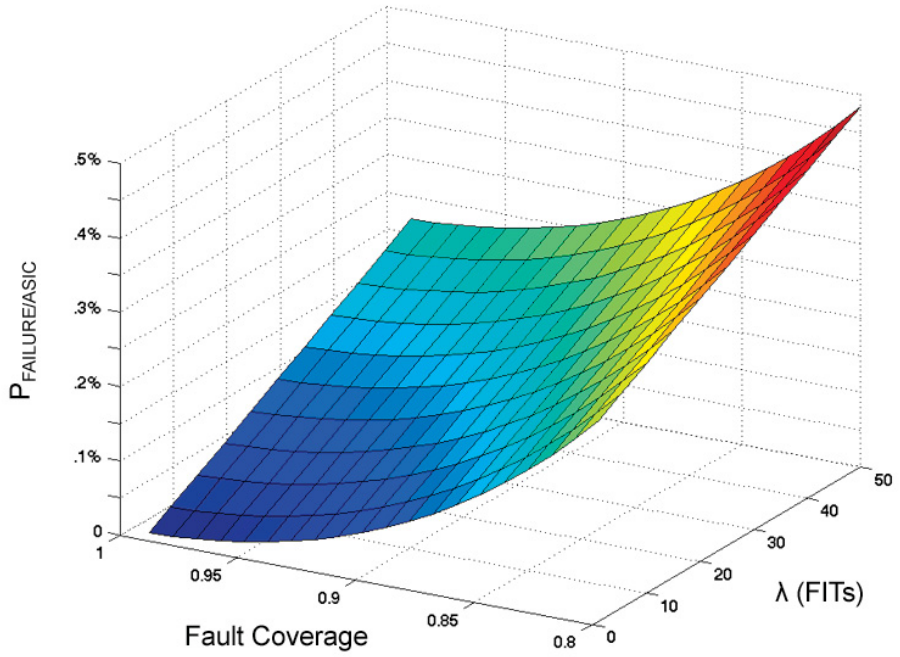

Figure 4-2. $P_{FAILURE/ASIC}$ versus fault coverage FC and useful life reliability λ for a 5-year mission.

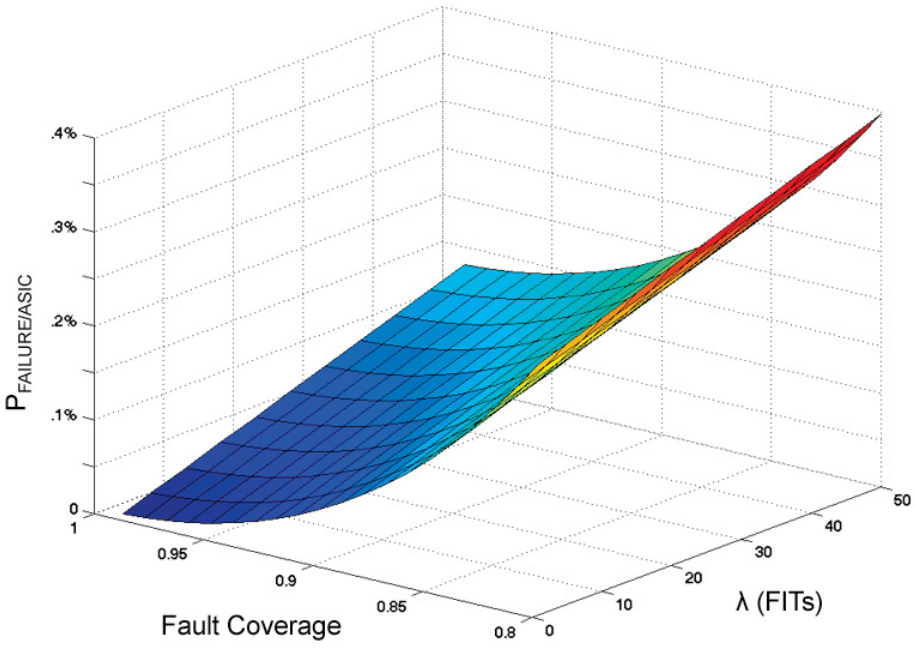

Figure 4-3. $P_{FAILURE/ASIC}$ versus fault coverage FC and useful life reliability λ for a 3-year mission.

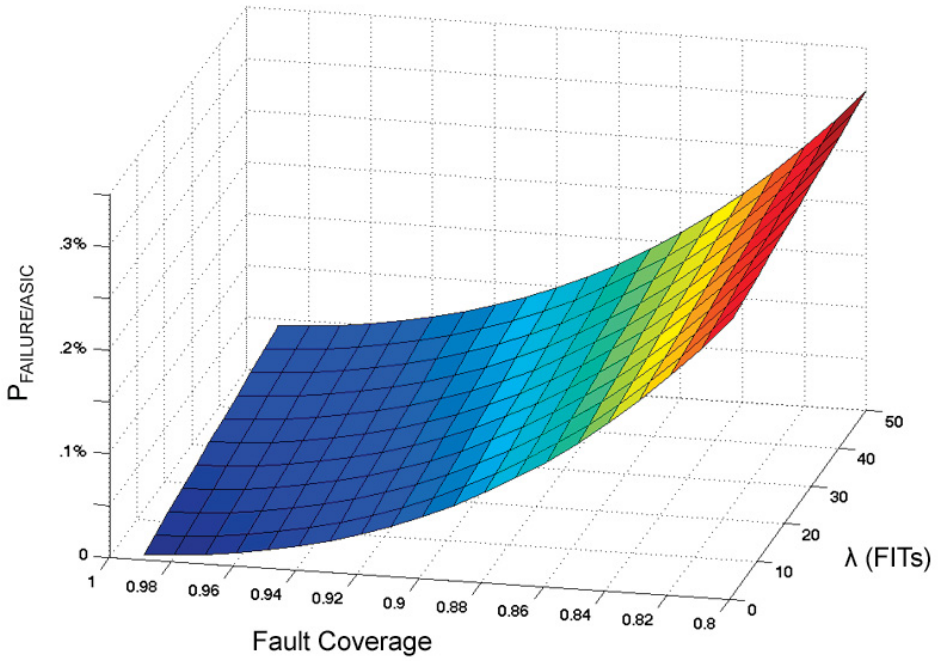

Figure 4-4. $P_{FAILURE/ASIC}$ versus fault coverage FC and useful life reliability λ for a 1-year mission.

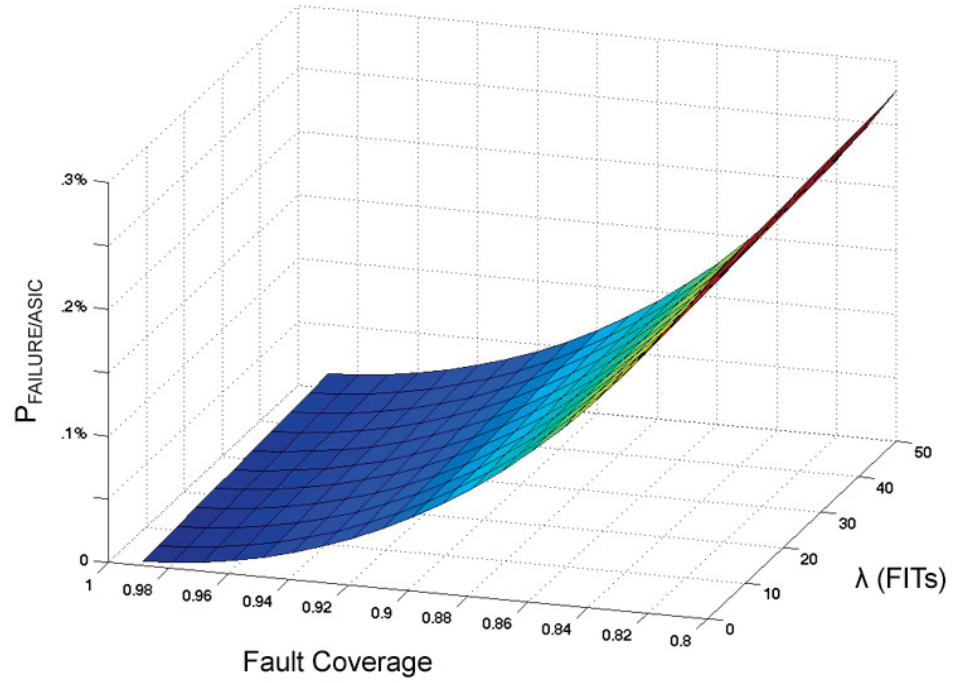

Figure 4-5. $P_{FAILURE/ASIC}$ versus fault coverage FC and useful life reliability λ for a 90-day mission.

4.3 System Reliability

Current space projects are still utilizing 0.25 μm CMOS processes for ASICs. For this reason, analysis can be further simplified by removing the variable λ and defining it to be 10 FITs. This number, in general, will be a good estimate for any mature CMOS ASIC technology.

Also, to be considered reliable enough for space application, it is assumed an ASIC system must have a reliability of 99%. This means less than 1% chance of failure due to defect or intrinsic failure mechanism (or radiation, which is not considered in this paper but can easily be added separately to the results presented herein) of any ASIC in the system.

Equation 9 gives the probability of ASIC system failure for m ASICs. Using this equation (after substituting Equation 8 for $P_{FAILURE/ASIC}$), a similar analysis can be performed to what was done previously for a single ASIC. However, this time, instead of varying FC and λ to see how $P_{FAILURE/ASIC}$ is affected, FC and m will be varied to see how $P_{FAILURE/SYS}$ is affected and where <1% chance of failure lies. Also, in this section, only fault coverage above 90% will be considered in order to achieve greater resolution in the figures. 90% fault coverage is considered bare minimum and analysis below that level is not necessary.

Figures 4-6 through 4-10 show probability of failure of a system of ASICs versus number of ASICs in the system and fault coverage. Tables 4-3 through 4-7 include the data points from these surface plots and state the maximum number of ASICs theoretically allowable to still achieve 99% reliability.

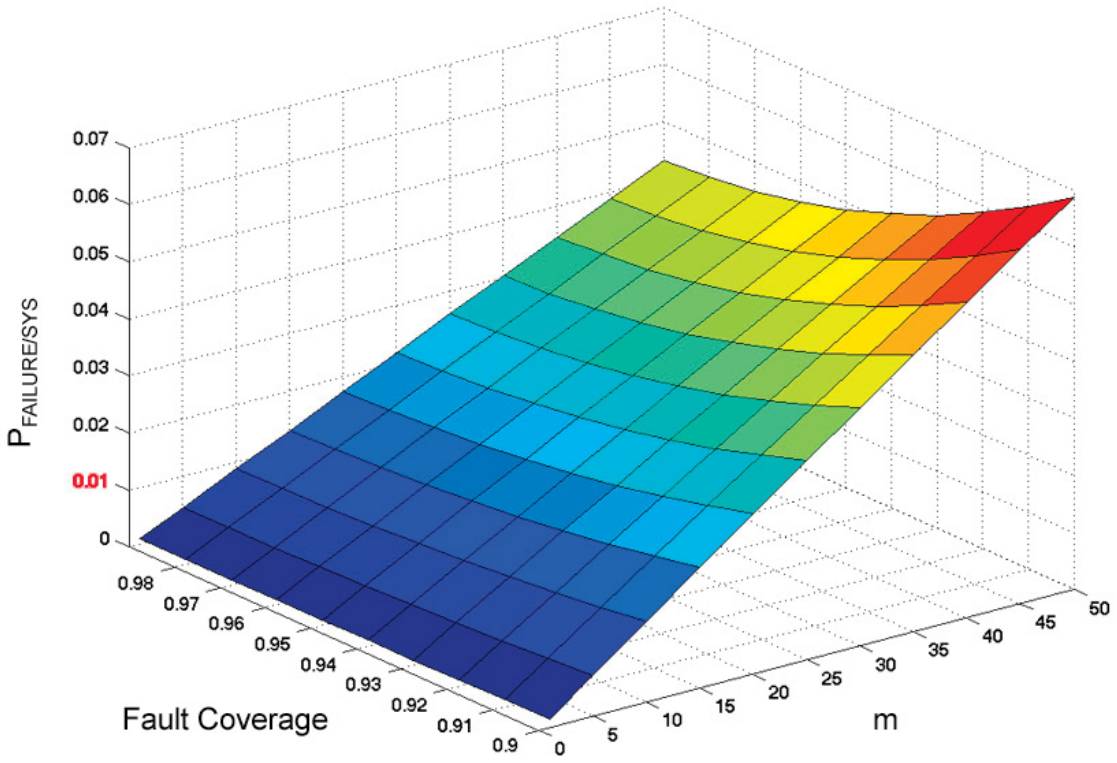

Figure 4-6. $P_{FAILURE/SYS}$ versus fault coverage FC and number of ASICs m for a 10-year mission (λ=10 FITs).

Table 4-3. Maximum number of ASICs for 99% system reliability for a 10-year mission (λ=10 FITs).

Fault Coverage (%)	Max # ASICs, *m*
99	11
98	11
97	10
96	10
95	10
94	9
93	8
92	8
91	7
90	7

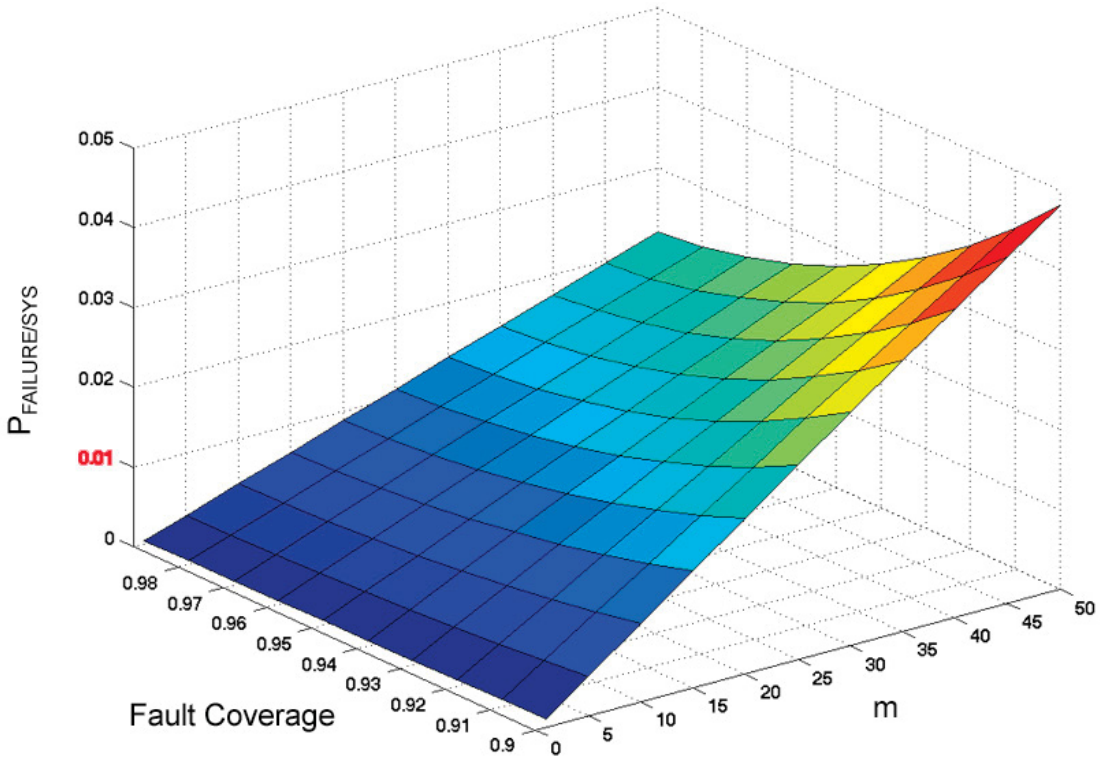

Figure 4-7. Probability of failure for a multi-ASIC system versus fault coverage and number of ASICs for a 5-year mission (λ=10 FITs).

Table 4-4. Maximum number of ASICs for 99% system reliability for a 5-year mission (λ=10 FITs).

Fault Coverage (%)	Max # ASICs, *m*
99	22
98	22
97	20
96	19
95	17
94	16
93	14
92	12
91	11
90	10

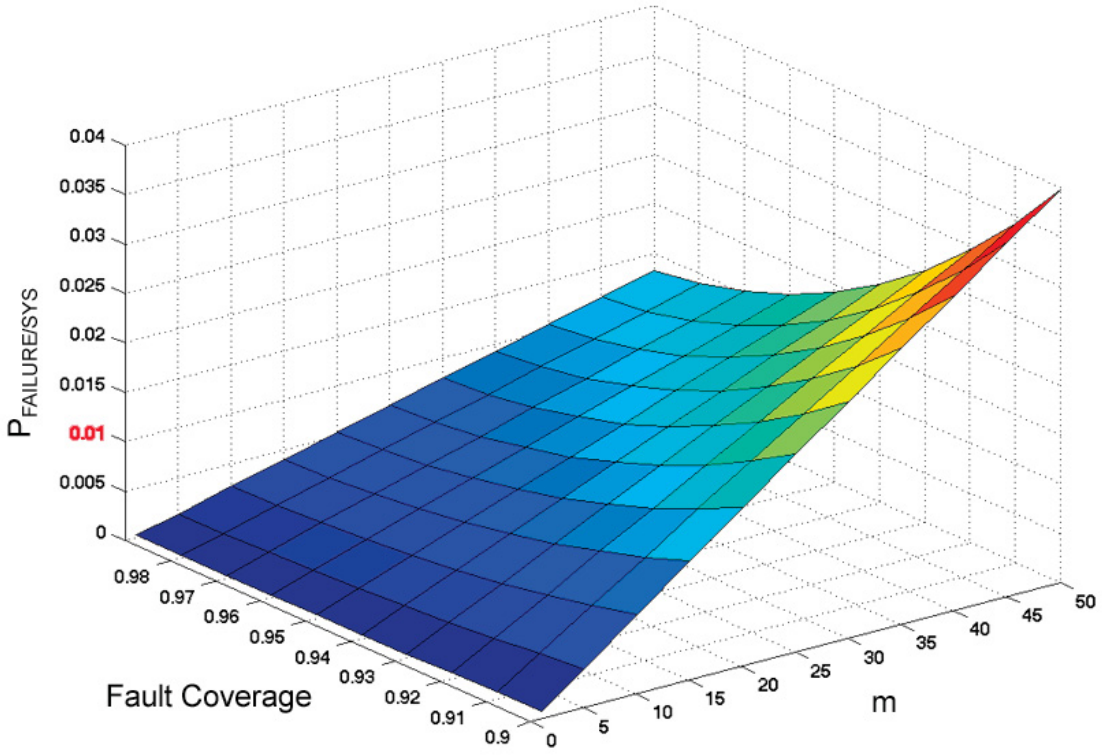

Figure 4-8. Probability of failure for a multi-ASIC system versus fault coverage and number of ASICs for a 3-year mission (λ=10 FITs).

Table 4-5. Maximum number of ASICs for 99% system reliability for a 3-year mission (λ=10 FITs).

Fault Coverage (%)	Max # ASICs, *m*
99	37
98	35
97	32
96	29
95	25
94	22
93	19
92	16
91	14
90	12

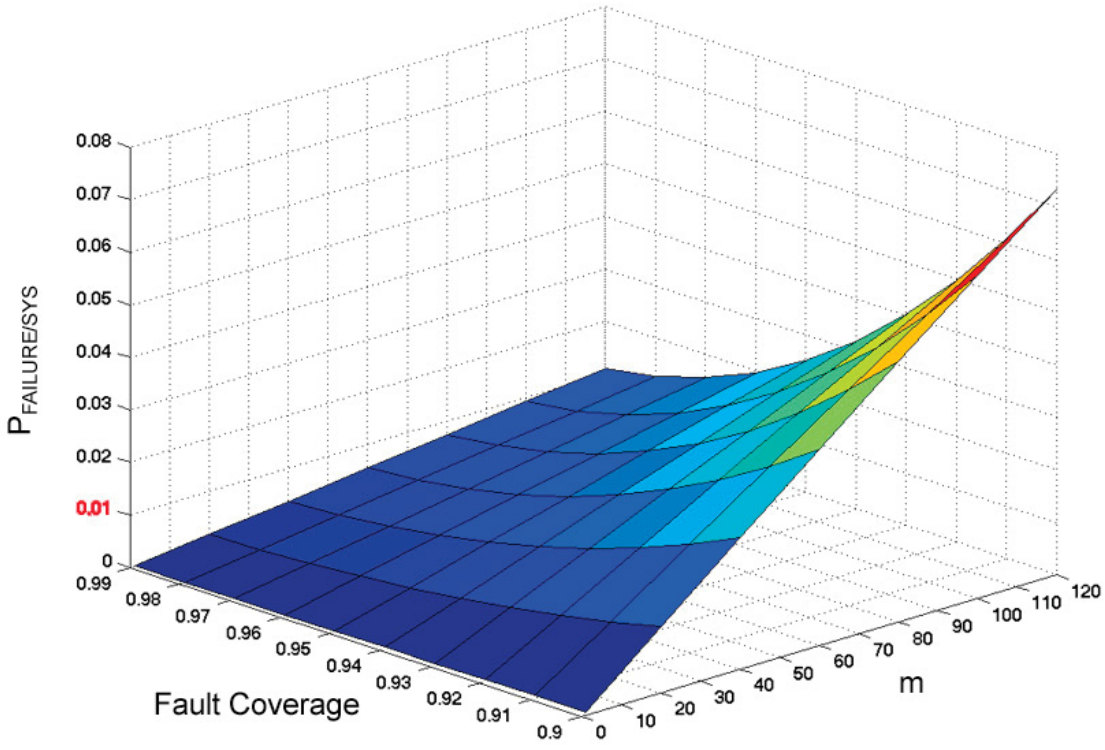

Figure 4-9. Probability of failure for a multi-ASIC system versus fault coverage and number of ASICs for a 1-year mission (λ=10 FITs).

Table 4-6. Maximum number of ASICs for 99% system reliability for a 1-year mission (λ=10 FITs).

Fault Coverage (%)	Max # ASICs, *m*
99	109
98	94
97	76
96	60
95	47
94	37
93	29
92	23
91	19
90	14

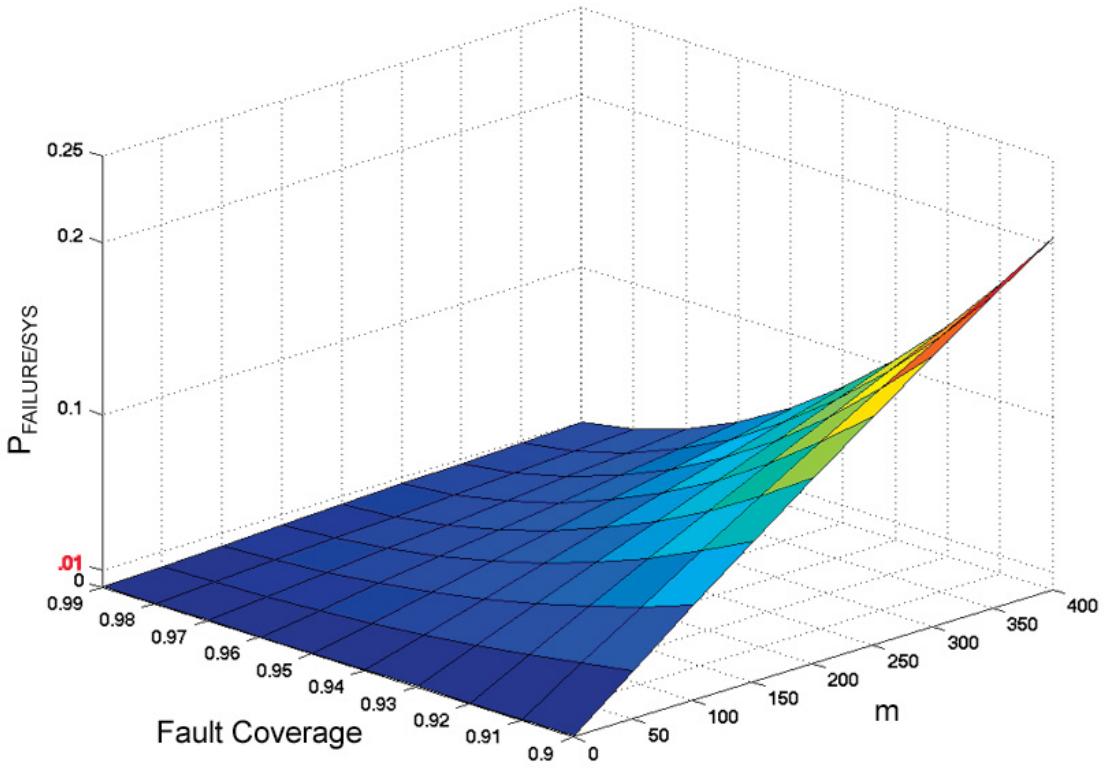

Figure 4-10. Probability of failure for a multi-ASIC system versus fault coverage and number of ASICs for a 90-day mission (λ=10 FITs).

Table 4-7. Maximum number of ASICs for 99% system reliability for a 90-day mission (λ=10 FITs).

Fault Coverage (%)	Max # ASICs, *m*
99	383
98	248
97	155
96	100
95	68
94	49
93	36
92	25
91	21
90	17

5.0 FAULT COVERAGE RECOMMENDATION FOR SPACE MISSIONS

The analysis presented here shows that for shorter mission durations, failure rates are dominated by extrinsic failure mechanisms, or defects. This is why the beginning portion of the bathtub curve is high but slopes steeply downward and flattens out during the useful life portion. For these shorter missions, fault coverage is more critical than the technology's determined useful-life failure rate λ. This is why Figure 4-5 (90-day mission) shows almost no change in probability of failure with changes in λ.

For longer mission durations, varying λ has a stronger impact on reliability than fault coverage. Figure 4-1 (10-year mission) shows probability of failure varying much more significantly with λ than fault coverage.

Figure 5-1 shows the maximum number of ASICs allowed in a system in order to achieve 99% reliability for various mission lifetimes (same assumptions: λ = 10 FITs, $Y = 0.75$, and $n_0 = 3$). Instead of requiring missions to have a specific level of fault coverage (e.g., 95% or 99%), missions should instead use the fault coverage necessary to achieve the required reliability for the number of ASICs in the system.

To properly calculate ASIC system reliability, many quantities must be considered, including die yield Y, useful life failure rate λ, average number of defects per defective die n_0, mission lifetime t, number of ASICs in the system m, and fault coverage FC. To facilitate making these calculations and to easily see how the results are affected by changing the variables, an ASIC system reliability calculator is provided at http://parts.jpl.nasa.gov/asic-calculator/.

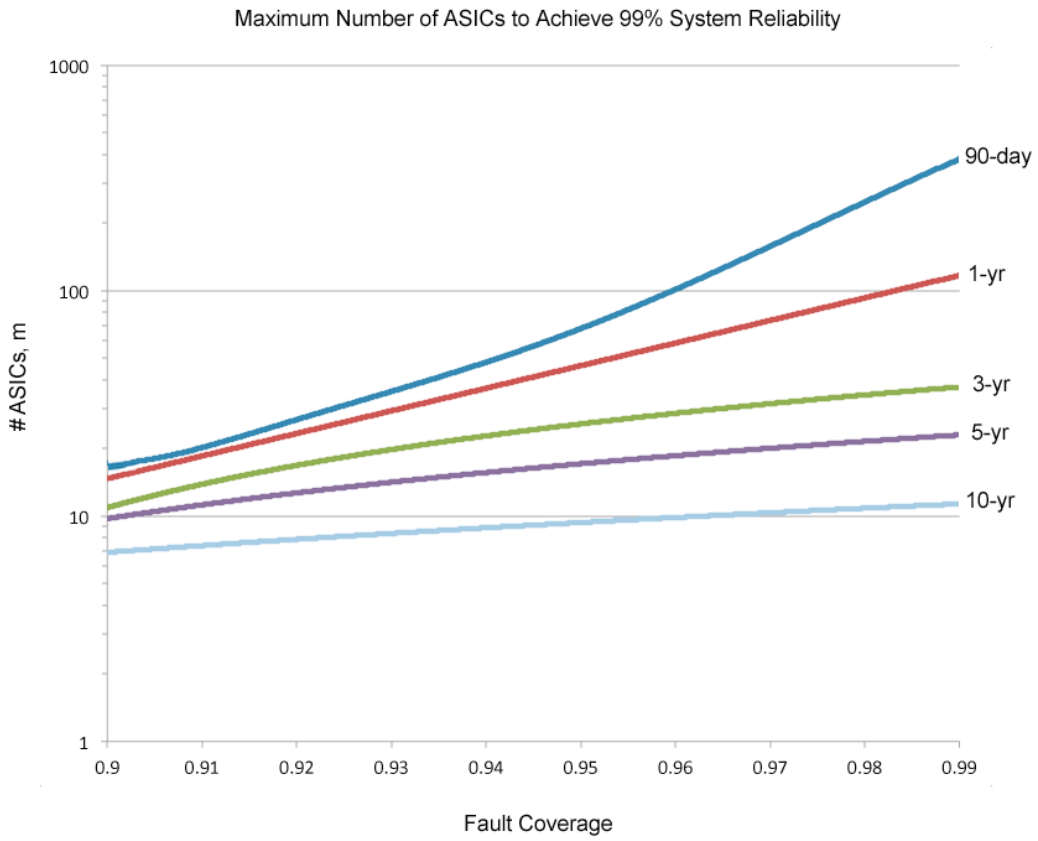

Figure 5-1. Maximum number of ASICs allowed to achieve 99% system reliability for a given mission lifetime and fault coverage (λ = 10 FITs, $Y = 0.75$, $n_0 = 3$).

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